1. A method for forming a metal layer in a via, comprising:

forming a metallic material on a surface of an insulator and within and over a bottom of the via;

forming a hard mask over the metallic material in the via;

removing the metallic material from the surface of the insulator; and

removing the hard mask from the via.

2. The method of claim 1, wherein said act of forming the hard mask comprises depositing a flowable oxide on the metallic material in the via.

3. The method of claim 2, wherein said act of depositing the flowable oxide is performed in a temperature range of 50 °C to 90 °C.

4. The method of claim 2, wherein said act of depositing the flowable oxide comprises depositing silicon oxide.

5. The method of claim 4, wherein said act of depositing the silicon oxide comprises chemical vapor depositing the silicon oxide.

6. The method of claim 2, wherein said act of depositing the flowable oxide comprises depositing a spin-on material.

7. The method of claim 1, wherein said act of forming the metallic material comprises depositing a silver film.

8. The method of claim 7, wherein said act of depositing the silver film comprises plasma vapor depositing silver to form the silver film.

9. The method of claim 1, wherein said act of removing the metallic material from the surface of the insulator comprises etching the metallic material from the surface of the insulator.

10. A method for making a programmable conductor random access memory, comprising:

forming a first conductor on the substrate;

forming an insulator on the substrate;

forming a via in the insulator extending to the first conductor;

forming a metallic material on a surface of the insulator and in the via in contact with the first conductor;

forming a hard mask over said metallic material within the via;

removing the metallic material from the surface of the insulator;

removing the hard mask;

forming a chalcogenide material in the via in contact with the

metallic material;

forming a metal-containing material in the via in contact with the chalcogenide material; and

forming a second conductor on the surface of the insulator and in contact with the metal-containing material.

11. The method of claim 10, wherein said act of forming the metallic material on the surface of the insulator and in the via comprises depositing the metallic material on the surface of the insulator and in the via.

12. The method of claim 11, wherein said act of depositing the metallic material comprises depositing a silver film.

13. The method of claim 10, wherein said act of forming the hard mask comprises depositing a flowable oxide on the metallic material in the via.

14. The method of claim 13, wherein said act of depositing the flowable oxide comprises depositing silicon oxide.

15. The method of claim 14, wherein said act of depositing the silicon oxide comprises chemical vapor depositing the silicon oxide.

16. The method of claim 10, wherein said act of forming the hard mask is performed in a temperature range of 50 °C to 90 °C.

17. The method of claim 10, wherein said act of forming the hard mask comprises depositing a spin-on material.

18. The method of claim 10, wherein said act of removing the metallic material from the surface of the insulator comprises etching the metallic material from the surface of the insulator.

19. The method of claim 10, wherein said act of forming the chalcogenide material in the via comprises depositing a chalcogenide glass in the via having a Ge_xSe_{100-x} stoichiometry.

20. The method of claim 19, wherein the Ge_xSe_{100-x} stoichiometry is in the range of $Ge_{20}Se_{80}$ to about $Ge_{43}Se_{57}$.

21. A programmable conductor random access memory intermediate structure, comprising:

a substrate;

a first conductor formed on said substrate;

an insulator formed on said first conductor, at least one via formed within said insulator and extending to said first conductor;

a metallic material formed in said at least one via; and

a hard mask formed on said metallic material within said at least one via.

22. The programmable conductor random access memory intermediate structure of claim 21, wherein said metallic material comprises silver.

23. The programmable conductor random access memory intermediate structure of claim 21, wherein said flowable oxide comprises silicon oxide.

24. The programmable conductor random access memory intermediate structure of claim 21, wherein said metallic material is deposited on a surface of said insulator.